

Claims

What is claimed is:

1 1. A method, comprising:
2 asserting an edge-triggered interrupt signal to a processor; and
3 delivering an interrupt pending signal from the processor to a power management
4 device.

1 2. The method of claim 1, further comprising the power management device
2 causing the processor to enter a high power state if the processor is in a low power state
3 when the processor delivers the interrupt pending signal to the power management
4 device.

1 3. The method of claim 2, wherein delivering an interrupt pending signal
2 includes delivering the interrupt pending signal from the processor to the power
3 management device over a single signal line coupled between a single processor pin and
4 the power management device.

1 4. The method of claim 3, wherein causing the processor to enter a high
2 power state includes the power management device deasserting a stop clock signal.

1 5. A method, comprising:
2 asserting an edge-triggered interrupt signal to a processor;

3 setting a bit within the processor indicating that an interrupt is pending; and
4 polling the processor to determine if an interrupt is pending.

1 6. The method of claim 5, wherein polling the processor to determine if an
2 interrupt is pending includes polling the processor to determine if an interrupt is pending
3 only if the processor is in a low power state.

1 7. The method of claim 6, further comprising causing the processor to enter a
2 high power state if the polling of the processor reveals that an interrupt is pending.

1 8. The method of claim 7, wherein causing the processor to enter a high
2 power state includes deasserting a stop clock signal delivered from a power management
3 device to the processor.

1 9. A system, comprising:
2 a processor including a local interrupt controller and an interrupt pending signal
3 output;
4 an input/output interrupt controller coupled to the processor, the input/output
5 interrupt controller to deliver an edge-triggered interrupt signal to the processor; and
6 a power management device including an interrupt pending signal input coupled
7 to the interrupt pending signal output of the processor, the processor to assert the interrupt
8 pending signal in response to the delivery of the edge-triggered interrupt signal.

1 10. The system of claim 9, wherein the processor further includes a stop clock
2 signal input, the processor to cease executing instructions in response to an assertion of
3 the stop clock signal by the power management device.

1 11. The system of claim 10, the power management device to cause the
2 processor to enter a high power state if the processor is in a low power state when it
3 asserts the interrupt pending signal.

1 12. The system of claim 11, wherein the power management device causes the
2 processor to enter the high power state by deasserting the stop clock signal.

1 13. A power management device, comprising:
2 an interrupt pending signal input, an assertion of the interrupt pending signal to
3 indicate that a processor has an interrupt pending; and
4 a processor power management signal output, the power management device to
5 cause the processor to enter a high power state by signaling to the processor to enter the
6 high power state via the processor power management signal if the processor is in a low
7 power state when it asserts the interrupt pending signal.

1 14. The power management device of claim 13, wherein the processor power
2 management signal is a stop clock signal, and further wherein the power management
3 device causes the processor to enter a high power state by deasserting the stop clock
4 signal.

